Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.028”**

**D**

**G**

**G**

**S**

**F450**

**.028”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035 x .0035”**

**Backside Potential:**

**Mask Ref: F450**

**APPROVED BY: DK DIE SIZE .028” X .028” DATE: 2/26/20**

**MFG: INTERFET THICKNESS .008” P/N: 2N6550**

**DG 10.1.2**

#### Rev B, 7/1